IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A weighting circuit for a receiver which is provided for receiving a multicarrier signal comprising carrier signals, comprising:

a memory storing a plurality of weighting coefficient sets,

a selector selecting one of the plurality of weighting coefficient sets stored in the memory on the basis of an expected spurious signal energy in the received signal, and

an estimation unit calculating said expected spurious signal energy using a first cross-correlation between the received signal and at least one spurious signal to be expected, and a second cross correlation between the received signal and a spurious signal to be expected, which has been phase-shifted through 90 degrees;

wherein the weighting circuit weights the carrier signal such that the spurious signal energy is of equal magnitude for all weighted carrier signals;

wherein said expected spurious signal energy is set externally; [[and]]

wherein the memory is programmable via an external interface connected to said memory though a plurality of internal data lines, and

wherein the programmable memory is connected to the selector via a plurality of address lines, the selector being capable of selecting a particular weighting coefficient set from the plurality of weighting coefficient sets stored within the memory.

2. (Previously Presented) The weighting circuit as claimed in claim 1, wherein the weighting circuit has at least one multiplier which multiplies an associated carrier signal by a stored weighting coefficient from the selected weighting coefficient set.

3. (Canceled)

4. (Previously Presented) The weighting circuit as claimed in claim 1, wherein the multicarrier signal is broken down into the carrier signals by a computation circuit.

5. (Previously Presented) The weighting circuit as claimed in claim 4, wherein the computation circuit is a Fast Fourier Transformation circuit.

6. (Previously Presented) The weighting circuit as claimed in claim 5, wherein the carrier signals broken down by the computation circuit are buffer-stored in a buffer store.

7-12. (Canceled)